Abstracts

5-GHz CMOS wireless LANs

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This paper first provides an overview of some recently ratified wireless local-area network (WLAN) standards before describing an illustrative 5-GHz WLAN receiver implementation. The receiver, built in a standard 0.25-/spl mu/m CMOS logic technology, exploits several recent developments, including lateral-flux capacitors, accumulation-mode varactors, injection-locked frequency dividers, and an image-reject low-noise amplifier. The receiver readily complies with the performance requirements of both IEEE 802.11a and ETSI HiperLAN. It exhibits a 7.2-dB noise figure, as well as an input-referred third-order intercept and 1-dB compression point of -7 and -18 dBm, respectively. Image rejection for this double conversion receiver exceeds 50 dB throughout the frequency band without using external filters. Leakage out of the RF port from the local oscillators is under -87 dBm, and all synthesizer spurs are below the -70-dBm noise floor of the instrumentation used to measure them. The receiver consumes 59 mW from a 1.8-V supply and occupies only 4 mm/sup 2/ of die area, in no small measure due to the use of fractal capacitors for ac coupling.

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